ADJUSTABLE GAIN PRECISION FULL WAVE RECTIFIER WITH REDUCED ERROR

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to circuitry for conditioning alternating current waveforms to produce amplified and rectified waveforms. In particular, the invention relates to a technique for receiving AC waveforms of a fairly large dynamic range, rectifying the waveform, and amplifying the waveform by one of a plurality of discrete gain levels in a closed loop feedback configuration for obtaining waveforms suitable for input into downstream circuitry, such as an analog-to-digital converter.

2. Description Of The Related Art

A variety of applications exist for signal processing of alternating current waveforms wherein the input waveform must be rectified and amplified for application to downstream circuitry. For example, in a current sensing relay, current sensors may be applied to one or more current-carrying conductors for outputting signals which are indicative of a level of current flow. Depending upon the type of downstream processing, the signal may need to be rectified and digitized, particularly where downstream circuitry includes digital signal processing circuitry such as microprocessors, digital signal processors, and the like. In such arrangements, circuitry must not only rectify the input signal, but may need to amplify the input signal to make best use of the dynamic range of an analog-to-digital converter. The amplification becomes somewhat more complex in applications where the dynamic range of the input signal itself may vary widely.

In applications including analog-to-digital converters and input signals comprising AC waveforms of a broad dynamic range, difficulties may be encountered in the scaling of the rectified waveform to make best use of the dynamic range of the analog-to-digital converter, while avoiding excessive amplification of noise. For example, where an input signal to such circuitry is an AC waveform, a very low amplitude may result in output data from the analog-to-digital converter which is of little utility due to a lack of sufficient amplification. On the contrary, where an input signal has a dynamic range which may change substantially during operation, a fixed amplification level may cause the analog-to-digital converter output to saturate when the amplitude of the input signal increases substantially as compared to its normal amplitude levels, or at least to the amplitude levels at which the amplification gain was appropriate.

In monitoring and control equipment, such as microprocessor-based overload relays, very substantial dynamic ranges may be encountered in input levels of AC waveforms, such as from current sensors. To perform analysis of the input signals, however, the signals must be rectified and digitized. Accommodation of the large variations in the amplitude of the input signal requires a novel approach to both the rectification and the amplification of the signal prior to application of the output to the analog-to-digital converter.

In general, analog-to-digital converters may not sample negative portions of an input signal, such devices generally operating between an input range of 0 to 5 volts. Thus, precision full wave rectifiers are typically needed to provide an absolute value function, affording proper operation of the analog-to-digital converter. Traditional full wave rectifiers have been employed for this purpose, including a pair of cascaded amplifiers to produce the absolute value function. However, such devices often produce intolerable levels of error due to the amplification of the first stage amplifiers error by the second amplifier, and addition of this amplified error to the error of the second amplifier itself. Moreover, conventional precision full wave rectifiers may offer gain, but do not offer adjustable gain. Such adjustability in gain levels would be highly desirable to

increase the dynamic range of the system, but such adjustability is difficult to synthesize in a non-cascaded amplifier approach.

5   There is a need, therefore, for a technique capable of rectifying and amplifying AC waveforms of varying amplitude. For practical applications, the technique should be relatively easy to implement and cost effective to manufacture. Moreover, there is a particular need for a technique which provides discrete levels of amplification based upon the level of an output waveform applied to downstream circuitry, such as an analog-to-digital converter. In circuits including a digital signal processor, a microprocessor or a

10   similar programmable device, it would be particularly convenient to provide some degree of feedback control of the amplification level based upon detected and fed-back characteristics of the output waveform.

15

SUMMARY OF THE INVENTION

20   The present invention provides a technique for rectifying and amplifying an input waveform designed to respond to these needs. The technique may be implemented in a variety of devices, but is particularly well suited to devices in which an input waveform has a substantial dynamic range, requires rectification, and must be amplified to optimize a dynamic range of downstream circuitry. The technique makes use of inverting and non-

25   inverting amplifier circuits, such that rectification is performed by inverting negative polarity lobes of an input waveform, while passing positive polarity lobes without inversion. Amplification is performed by both the inverting and the non-inverting circuits. The gain of each of the amplifying circuits may be selected among a plurality of discrete gains as defined by a switchable resistance circuit associated with each amplifier. In a

30   preferred configuration, solid state switches are employed for selecting the appropriate gain level.

4

Where a microprocessor or other programmable digital signal processing circuitry is employed in the device, the discrete gain may be selected by detecting the amplitude of the waveform, or of a digitized signal downstream of the amplifiers. The output signal

5   amplitude, or the output of an analog-to-digital converter receiving the rectified and amplified signal is fed back to the microprocessor, which then generates command signals for placing the selector switches in conductive states appropriate for selecting the desired gain. Various schemes may be employed for selecting the appropriate gain. In a presently preferred configuration, for example, the circuitry may assume and lowest gain level,

10   monitor output, and increase gain until the output reaches a level that does not saturate the downstream circuitry, particularly an analog-to-digital converter. The input signal is thus rectified, and amplified to make optimal use of the dynamic range of the downstream circuitry.

15

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

20

Figure 1 is a diagrammatical representation of a feedback loop for selecting and controlling gains in a rectifying and amplifying circuit in accordance with certain aspects of the present technique;

25   Figure 2 is a diagrammatical representation of certain of the functional circuits comprising the rectification and amplification circuits of the arrangement of Figure 1, as well as selector and control circuitry for selecting among discrete gain levels; and

Figure 3 is a schematic representation of a presently preferred circuit for carrying

30   out the rectification and selective amplification functions implemented via the functional circuitry of Figure 2.

5

4

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

Turning now to the drawings, and referring first to Figure 1, a signal conversion

5   circuit, designated generally by the reference numeral 10, is illustrated for converting an AC
waveform as an input signal to a rectified and amplified output waveform. Signal
conversion circuit 10 includes a rectifier circuit with gain 12, an analog-to-digital (A/D)
converter circuit 14, and a selector/control circuit 16. The rectifier circuit 12 receives an
input as indicated at reference numeral 18. The input waveform, shown graphically at

10   reference numeral 20, may generally be an AC waveform, such as a waveform produced by
a sensor. In a present embodiment, the input waveform is produced by a current sensor
associated with an AC conductor (not shown). However, other waveform sources and types
may be applied to circuitry 10. The input waveform 20 has an amplitude 22 which may
vary substantially during operation. By way of example, in a present application, an input

15   waveform may vary in amplitude from a level of approximately 10mv to approximately
2.5v. Circuit 12, which includes components for selectively applying one of a plurality of
discrete gains, rectifies the input signal, and amplifies the input signal to produce an output
waveform along an output 24.

20   The output waveform, designated generally by reference numeral 26 in Figure 1, is
rectified and preferably amplified to obtain an amplitude which optimizes the dynamic
range of downstream circuitry, such as A/D converter 14. In a presently contemplated
application, the A/D converter 14 may receive signals of levels of between 0 and 5v, but
optimally receives input signals along line 24 resulting in output counts from the A/D

25   converter of desired levels (e.g. 65 to 235 counts of a 255 count range), corresponding to
input voltages of similar levels (e.g. approximately 1 volt and 4.5 volts). As will be
appreciated by those skilled in the art, the actual A/D count output will generally vary with
both the input voltage and current to the A/D converter. Switching of the discrete gains, as
described below, may actually be performed at various range levels or average levels, and

30   the particular switching levels may differ depending upon whether gain is being increased
or decreased, to provide stabilizing hysteresis in switching between gain levels.

To accommodate the dynamic range needed by A/D converter 14, circuitry 10 selectively applies gain levels in rectifier circuit 12 under the control of selector/control circuit 16. Selector/control circuit 16, to implement this selection function, receives

5   feedback of the output via a feedback line 30. Feedback to the selector/control circuit 16 may be in the form of a rectified, amplified waveform, but in the illustrated embodiment, is actual output from the A/D converter 14. In particular, where a digital circuit, such as a microprocessor is employed with appropriate code for carrying out the selection and control functions of circuit 16, a digitized signal may be conveniently applied to the circuit for

10   analysis of the appropriate amplification level and control as described below. Based upon the level of the feedback signal, circuit 16 produces command or control signals and applies them to circuit 12 as indicated at line 32. Finally, based upon the appropriate amplification level, A/D converter 14 produces a digital output signal as indicated at reference numeral 34, which is applied to downstream circuitry for the desired signal analysis, control, and

15   other functions.

Figure 2 illustrates functional circuitry components of the signal conversion circuitry 10 in somewhat greater detail, particularly of the rectifier circuit with gain 12. As shown in Figure 2, circuit 12 receives input via input line 18, and routes the input to a pair

20   of amplifier circuits 36 and 38. Circuit 36 is an inverting amplifier circuit with selectable gain. Circuit 36 converts negative polarity lobes of the input signal to positive polarity lobes, and applies a selectable gain to the rectified signal portions for output along output line 24. Circuit 38, conversely, is a non-inverting amplifier with selectable gain. Circuit 38 thus passes positive polarity lobes of the input waveform, applying a selected gain to the

25   positive lobes, also for output along output line 24. The output line thus carries rectified and amplified output waveforms comprising combinations of the output of circuits 36 and 38. Feedback to the selector/control circuit 16 is provided via feedback line 30, which as indicated above, may be based upon digital output from a downstream A/D converter.

30   Circuits 36 and 38 include amplifiers and resistance selection circuitry for applying one of a plurality of discrete gain levels to the input waveform. In particular, inverting

amplifier circuit 36 includes an inverting amplifier 40 with a feedback resistance selection circuit 42. Because the input resistance to inverting amplifier 40 is known and constant, gain of the inverting amplifier may be controlled by appropriately selecting the resistance of feedback resistance selection circuit 42, and summing the feedback and input signals as

5   indicated in Figure 2. Similarly, non-inverting amplifier circuit 38 includes a non-inverting amplifier 44. However, because amplifier 44 is non-inverting, control of the gain of the amplifier is selected via an input resistance selection circuit 46, with a constant and known feedback resistance being provided. As will be appreciated by those skilled in the art, the effective gains of amplifier circuits 36 and 38 are established by relationships between the

10   feedback and input resistances. Variations on the circuitry illustrated in Figure 2, and discussed in greater detail below with reference to Figure 3, may be envisioned, in which some or all of the adjustment in gain is made via regulation of both feedback and input resistance levels on both the inverting and non-inverting amplifiers. However, the preferred embodiment illustrated benefits from a reduced number of components and a

15   straightforward implementation.

       Figure 3 illustrates the inverting and non-inverting amplifier circuits with selectable discrete gains in somewhat greater detail. In particular, rectifier circuit with gain 12 includes the inverting amplifier 36 and the non-inverting amplifier 38 comprised of

20   operational amplifiers, including an inverting amplifier 40, and a non-inverting amplifier 44. An input resistance 48 is coupled to an input line 50 to inverting amplifier 40 to provide the desired input resistance for gain control. In a present embodiment, resistance 48 has a value of 4.99 kohms. A compensation resistor 52, such as a 4.87k ohm resistor is coupled between input 54 of inverting amplifier 40 and an analog ground potential, defining a low

25   impedance connection to ground. Amplifier 40 is further coupled to power supply sources 56 and 58, such as a positive and negative 12 volt bus. The power supply line 56 may be further connected to an analog ground potential through a decoupling capacitor 60. In the illustrated embodiment, because a dual operational amplifier package is employed, a single pair of capacitors 60 (and 90 described below) are used. Other component packaging may

30   require additional decoupling capacitors. Where desired, a tuned resistance may be provided in place of resistor 52 to reduce voltage errors at output line 24.

Output 62 of inverting amplifier 40 is coupled to a diode pair 64 on output line 24 to maintain the amplifier in an off state when non-inverting amplification circuit 38 is functional in applying an output signal. The diode pair thus includes one diode operational

5   as a shunt between the amplifier's inverting terminal and its output, and a blocking diode between the amplifier's output and outline line 24. The output of inverting amplifier 40 is further coupled to feedback resistance selection circuit 42 which serves to place a desired resistance value along the feedback line of the amplifier to control the amplifier gain. Circuit 42 includes a low pass noise filtering capacitor 66 in parallel with a first feedback

10   resistor 68. In parallel with resistor 68, at least one additional selectable resistance is provided, two such resistances being provided in the illustrated embodiment and designated by reference numerals 70 and 72. Resistances 70 and 72 may be selectively coupled in parallel with resistance 68 via a solid state switches 74 and 76, such as n-channel MOSFETs. While any desired resistances may be provided in the feedback portion of the

15   circuitry, in a presently preferred configuration, resistor 68 has a value of 165k ohm, resistor 70 has a value of 18.2k ohm, and resistor 72 has a value of 110k ohm. The solid state switches 74 and 76 are placed in a normally non-conducting state, and may be switched to a conducting state, thereby placing resistances 70 and 72 in parallel with resistance 68 (and with one another) by application of a control signal to gate input lines 78 of each switch.

20   Such command signals are provided by circuit 16 discussed above, which will preferably include a microprocessor or similar digital, configurable circuitry.

Input via input line 18 is transmitted to non-inverting amplification circuit 38 through a compensation resistor 80 and a noise filtering capacitor 82 coupled to an analog

25   ground potential. The input is then applied to non-inverting amplifier 44 as indicated at reference numeral 84. In a present embodiment, compensating resistor 80 has a value of 3.01 kohms, while capacitor 82 has a rating of 0.018 microF. Non-inverting amplifier 44 is coupled to a power source via inputs 86 and 88, such as positive and negative 12 volt bus lines. A decoupling capacitor 90 is coupled to negative power input 88 and to an analog

30   ground potential.

An output line 92 of non-inverting amplifier 44 is coupled to a diode pair 94 which insures that non-inverting amplification circuit 38 is off when a signal is being provided by inverting amplification circuit 36 along output line 24. Thus, like diode pair 64, diode pair 94 includes one diode operational as a shunt between the amplifier's inverting terminal and its output, and a blocking diode between the amplifier's output and out line 24. In parallel with the diode pair, a feedback resistor 96 is provided which establishes the feedback resistance level used to set the gain of circuit 38 in combination with the selections made in input resistance selection circuit 46. In a present embodiment, resistor 96 has a value of 95.3 kohms. Diode pair 94 and resistor 96 are then coupled to a negative input 98 of non-inverting amplifier 44.

Input resistance selection circuit 46 is coupled to negative input 98 of amplifier 44 and serves to selectively place one or more resistors in series between input 98 and an analog ground potential. In particular, in the illustrated embodiment, circuit 46 includes a first resistor 100 which is resident in the input line, as well as additional resistors 102 and 104 which may be selectively coupled in series with resistor 100 by opening solid state switching devices 106 and 108, respectively. In a present embodiment, resistor 100 has a rating of 3.01 kohms, resistor 102 has a rating of 38.3 kohms, and resistor 104 has a rating of 4.75 kohms. Switching devices 106 and 108 serve as gain selector switches, and are preferably n-channel MOSFETs. Inputs to the switching devices 106 and 108 are provided via gate input lines 110, coupled to selector/control circuit 16. Thus, circuit 16 may close switches 106 and 108 to create a parallel current-conducting path around each input resistor 102 and 104, or may open the switching devices to interrupt the parallel path and thus force all current flow through the resistors in series with input resistor 100.

As will be appreciated by those skilled in the art, the foregoing circuitry allows for inversion of the input waveform applied to input line 18. In particular, positive polarity portions of the waveform are transferred through circuit 38, with the positive portions of the waveform being amplified by the gain defined by the relationship:

$$G_{non\text{-}inverting} = (1 + R_{fb}/R_{input}) \qquad (eq.1);$$

9 10

where G is the effective gain of the circuit, R_{fb} is the feedback resistance defined by resistor 96, and R_{input} is the effective resistance defined by the network of circuit 46. Similarly, negative polarity portions of the input waveform are inverted by amplifier 40, with the

5   corresponding input waveform portions being amplified in accordance with the relationship:

$$G_{inverting} = R_{fb}/R_{input} \qquad (eq.\ 2);$$

where G is the gain of circuit 36, R_{fb} is the effective resistance of the network of circuit 42,

10   and R_{input} is the input resistance defined by resistor 48.

As mentioned above, various approaches may be employed with circuit 12 to command the discrete gain levels defined by the input and feedback resistance networks. In a presently preferred embodiment, output of the A/D converter 14 is monitored by the

15   selector/control circuit 16 and gain is first selected at a lowest level. If the output of the A/D converter is within a low region of the dynamic range of that device, circuit 16 commands switching devices 74, 76, 106 and 108 to increase the gain until the dynamic range is properly utilized. During operation, the output of the circuitry may be continuously monitored to adjust the gain to one of the discrete levels as desired. In the foregoing device,

20   three such discrete gain levels are provided, of approximately 2, 10 and 30. However, more or fewer discrete gain levels may be programmed, and these may be obtained through switching of solid state devices similar to the technique described above.

While the invention may be susceptible to various modifications and alternative

25   forms, specific embodiments have been shown and described herein by way of example only. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

30